JATAN VIJAYKUMAR MANDALIYA

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EDUCATION

San Francisco State University, San Francisco, CA — May 2026
Master of Science, Electrical and Computer Engineering — GPA: 3.7/ 4.0
Courses: Digital VLSI Design, ASIC Design, Advance Digital Design, Hardware for Machine Learning

Gujarat Technological University, Ahmedabad, India — May, 2024
Bachelor of Engineering, Electronics and Communication — GPA: 3.76 / 4.0
Courses: Digital System Design, Analog Circuit Design, VLSI Design, Testing and Verification

WORKING EXPERIENCE

Tirex Chargers — Jan 2024 – May 2024
Embedded Hardware Intern — Ahmedabad, India

- Designed hardware boards (PCB) for EV chargers using Altium, focusing on power and load regulation. Achieved 15% smaller board size by component placement and routing. also synthesized UPS logic using Op-Amps.
- Debugged boards, resolving 20+ design flaws (signal integrity, power sequencing, thermal management), maximized system stability by 20%, and verified voltage/current levels for compliance using oscilloscopes and spectrum analyzers.
- Simulated Buck and Boost converters with PI control in MATLAB/Simulink, and applied Machine Learning (ML) to accelerate parameter sweeps for optimizing efficiency and KPIs ensuring <5% noise and stable load regulation.

Nano – Electronics and Computing Research Lab - SFSU — Jan 2025 – Present
Graduate Research Assistant — San Francisco, CA

- Developed a Python framework to automate Spice simulations for distributed RC networks, enabling efficient extraction of propagation delay, slew rate, and tail characteristics under varying resistance, capacitance, and segment configurations.
- Implemented an admittance propagation algorithm to generate reduced-order RC interconnect models (Pi Model), achieving less than 5% error compared to full RC network simulations.
- Performed transient and data sweep analyses in HSPICE to benchmark the accuracy of reduced-order Pi models against full RC tree models for interconnect delay estimation, identifying cases where higher-order models are needed.

SKILLS

- **Programming Language:** Verilog, System Verilog, VHDL, TCL, Perl, Embedded C, C, C++, Assembly, Python.
- **Design Automation Tools:** Synopsys Custom Compiler (Similar to Cadence Virtuoso), VCS, IC Compiler (ICC2), LTSpice, PrimeTime, HSpice, WaveView, Design Compiler, Xilinx ISE, MATLAB, MultiSim, Proteus, Linux, Altium.
- **Computer Architecture:** RISC-V, Cortex-M, x86, Atmel AVR, 8085, 8051.
- **Communication Protocol:** UART, I2C, SPI, USB, CAN, RF (BLE, Wi-Fi), TCP/IP.
- **Other Skills:**, Machine Learning, FPGA, Soldering, SoC Design, PCB Design, Python scripting.

PROJECTS

Motion Estimator in 14nm CMOS | VCS, DC, PrimeTime, IC Compiler.

- Designed a Motion Estimator for video compression using the Block-Matching Algorithm, and engineered Verilog modules, including Processing Elements, Comparator, and Controller, with a pipelined architecture.
- Completed full RTL-to-GDSII, including synthesis, place-and-route, minimize area and power, and ECO for hold Violation.

16 x 18 SRAM Design using 14nm PDK | Custom Compiler WaveView.

- Constructed SRAM wrapper that includes Precharge circuit, write driver, Sense amp, Address Decoder & SRAM cell, created schematic and layout (optimized for area).
- Carried top-level functional verification, calculated and optimized for access time, and active power, cleared LVS & DRC.

MIPS32 Processor in 14nm CMOS | VCS, DC, PrimeTime, IC Compiler

- Built a 5-stage pipelined MIPS32 processor in Verilog, implementing fetch, decode, execute, memory, and write-back stages (including forwarding and hazard detection). Verified functionality using a testbench with assembly programs.
- Performed RTL to GDS. Simulated RTL, synthesized and mapped constraints, obtained GDS and implemented ECO.

Wireless Data Transmission and Communication Protocols on Spartan FPGA | Verilog, Xilinx.

- Integrated SPI and I2C communication protocols on Spartan FPGA for peripheral data exchange.
- Created a RF-based wireless data transmission between two FPGAs using SPI and the NRF24L01 transceiver.

Custom Standard Cell Library Design in 14nm Technology | Custom Compiler

- Developed individual layout for basic gates such as NAND, NOR, Inverter, XOR and verified timing properties.
- Tested timing characteristics under different temperatures using HSPICE simulations for pre- and post-layout analysis.
- Performed DRC, LVS, and parasitic extraction on each standard cell and created corresponding symbols.

CERTIFICATIONS

- VSD – Static Timing Analysis (Udemy)
- VSD – Clock Tree Synthesis (Udemy)
- Introduction to IoT (Cisco Networking Academy)